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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,158	09/26/2001	Martin Li	TI-33430	9577

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EXAMINER	
GREY, CHRISTOPHER P	
ART UNIT	PAPER NUMBER
2616	

NOTIFICATION DATE	DELIVERY MODE
07/29/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/964,158	LI ET AL.	
	Examiner	Art Unit	
	CHRISTOPHER P. GREY	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,7,10-14,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,4,5,7,18,19* is/are allowed.

6)☒ Claim(s) *10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 10-14, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen (US 6732206), in view of Holm (US 6122680).

Regarding Claim 10, Jensen discloses storing data cells from the ATM master processing unit **(Col 1 lines 65-66, master 10)** in a buffer storage unit **(Col 2 lines 12-13 FIFO)** coupled to the communication bus **(fig 1, 12, bus)**, wherein the buffer storage unit is a FIFO storage unit **(fig 1, 22)** configured to store two of the data cells **(Col 2 lines 29-31, capable of holding two cells)** to permit the data cells to be transferred on consecutive clock cycles to a destination location **(fig 2, U1 BUS transferring data from the cell FIFO on a clock cycle 8 BIT/16MHZ);**

Jensen discloses comparing a field in the data cell with the contents of a register to determine the destination location of each data cell **(Col 3 lines 7-16, where a CAM register is looked up in order to find a match/comparison to the first 2 words).**

Jensen discloses generating a signal identifying the destination location **(Col 3 lines 17-20, valid target port address);**

Jensen discloses a first READY signal **(Col 3 lines 41-45 and polling as described in Col 3 lines 26-27, where the status bit is equivalent to a READY signal as disclosed in the claim).**

Jensen does not specifically disclose when storage space is available, transferring a data cell from the buffer storage unit to the direct memory access unit, storing data cells in a output buffer unit received from the direct memory access unit in response to a second READY signal, where the output buffer unit is a first-in first-out storage unit and is configured to exchange control signals with the direct memory access unit; and receiving data cells at an output unit from the output buffer unit and applying data cells to the communication bus from the output unit, the output unit configured to exchange control signals with the ATM master processing unit.

Holm discloses when storage space is available, transferring a data cell from the buffer storage unit **(fig 1, 42 shows a FIFO)** to the direct memory access unit **(Col 4 lines 16-20, where data is retrieved from the RAM/FIFO, and transferred to the DMA 46 of fig 1)**, storing data cells in a output buffer unit **(fig 1, 40, shows an output buffer)** received from the direct memory access unit **(fig 1, 44 shows a DMA)** in response to a second READY signal **(Col 3 lines 59-60 shows a request signal equivalent to a 2nd ready signal),** where the output buffer unit is a first-in first-out storage unit **(fig 1, 40 shows a transmit FIFO buffer unit)** and is configured to exchange control signals **(fig 2, 150 and 151 are control signals exchanged b/w the FIFO and DMA according to Col 4 lines 61-66)** with the direct memory access unit **(fig 1, 44 shows DMA unit)**; and receiving data cells at an output unit **(fig 1, 30 is**

equivalent to an output unit) from the output buffer unit **(fig 1, 40 is equivalent to buffer unit)** and applying data cells to the communication bus **(fig 1, 50 shows communication bus)** from the output unit **(fig 1, 30 shows output unit),** the output unit **(fig 1, 30)** configured to exchange control signals **(fig 1, 50 and 52 shows that signals of some sort are exchanged)** with the ATM master processing unit **(fig 1, where 20 represents an ATM master processing unit similar to the one shown by Jensen).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the slave devices of Jensen, as taught by Holm, since stated in Col 1 lines 41-45, that such a modification will alleviate the difficulty to place a large number of RAM's on a single integrated circuit and no longer limit the number of communication channels that can be supported on the integrated circuit.

Regarding Claim 11, Jensen discloses transferring a data cell from the buffer storage unit to the ATM slave processing unit on consecutive clock cycles **(Col 2 lines 46-65 and figs 3 and 4, wherein the U1 TX state machine operates on a clock cycle, and allows the transmission of data from the FIFO).**

Regarding Claim 12, Jensen discloses implementing the signals exchanged over the communication bus in a UTOPIA format **(Col 1 lines 65-66).**

Regarding Claim 13, Jensen discloses applying the signal identifying the destination location to a target unit **(Col 3 lines 17-22, the comparison is determined to be valid, and the target CDP is polled, where this polling information is also equivalent tot eh signal identifying the destination).**

Jensen does not specifically disclose the target being a DMA.

Holm discloses the target being a DMA **(fig 1, 44 shows a DMA which is the target of write data incoming from the FIFO).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the slave devices of Jensen, as taught by Holm, since stated in Col 1 lines 41-45, that such a modification will alleviate the difficulty to place a large number of RAM's on a single integrated circuit and no longer limit the number of communication channels that can be supported on the integrated circuit.

Regarding claim 14, Jensen discloses an ATM master processing unit;

a communication bus coupled to the ATM master processing unit **(Col 1 lines 65-66, master 10)**;

an ATM slave processing unit **(fig 1, 14 shows slave units),**; and an ATM slave interface unit coupled to the communication bus **(fig 1, 12 shows a communication bus connected to a slave 14 and a master 10**), the slave interface unit including:

an input unit **(fig 2, GTL 16 55 is equivalent to an input unit),** the input unit exchanging UTOPIA format signals **(Col 1 lines 65-66, shows the capability of the devices to operate using the UTOPIA format)** with the ATM master processing unit **(fig 1, 10);**

an input buffer storage unit **(fig 2, 22, notice a FIFO is shown)**, the input buffer unit **(fig 2, 22, notice a FIFO is shown)** receiving data cell signals from the input unit

(fig 2, GTL 16 55 is equivalent to an input unit, and this unit sends data to the FIFO 22), the input buffer unit including:

a memory unit **(fig 1, see FIFO)**, the memory unit being a first-in/first-out storage unit **(fig 2, 22 shows specifically a FIFO)** configured to store two of the data cell signals **(fig 2, 22 shows that the FIFO is a 2 cell FIFO)** to permit the data cells to be transferred on consecutive clock cycles **(fig 2, U1 BUS transferring data from the cell FIFO on a clock cycle 8 BIT/16MHZ)** to a destination location **(fig 2, 26 shows possible destination locations)** when the destination location is available; and

a calculation unit **(fig 2, 36 is equivalent to a calculation unit);**

a register **(fig 1, 20, shows address translation unit equivalent to a register as it contains addresses),** the contents of the register identifying a destination location field **(Col 2 lines 14-16 shows that the header is used and address of destination is translated)** in a data cell **(Col 2 lines 15 shows header, which means that a data cell was received)**, the contents of the register providing the translation of the field in the data cell into a destination location **(fig 1, 20, address translation unit is clearly present for address translation),** wherein the calculation unit generates a destination location signal **(Col 3 lines 17-18, output/generate valid target port address)** and;

an output buffer unit **(fig 7, 422 shows an output buffer unit),** the output buffer unit being a first-in first-out storage unit **(fig 7, 422, notice FIFO)** for storing data cells **(fig 7, 422, where the FIFO is a 2 cell FIFO for storing 2 cells),**

Jensen does not specifically disclose the ATM slave processing unit including a direct memory access unit, the memory_ unit transferring the data cells to the direct memory_ access unit in response to a first READY signal, applies the destination location signal to the direct memory access unit, the output buffer unit receiving data cells from the direct memory access unit in response to a second READY signal and exchanging control signals with the direct memory access unit; and an output unit, the output unit receiving data cells from the output buffer unit and applying data cells to the communication bus, the output unit exchanging UTOPIA format signals with the ATM master processing unit.

Holm discloses the ATM slave processing unit **(fig 1 10 is equivalent to the slave unit disclosed in Jensen)** including a direct memory access unit **(fig 1, 44 notice DMA)**, the memory unit **(fig 1, 42 shows a memory unit)** transferring the data cells to the direct memory access unit **(fig 7 shows data being received in the FIFO and transferred to the DMA)** in response to a first READY signal **(Col 4 lines 15-16, where the grant is equivalent to a 1st READY signal),** applies the destination location signal to the direct memory access unit **(fig 6, 246, where an address location signal is sent to a RAM, where a RAM is a form of DMA)**, the output buffer unit **(fig 1, 40, shows an output buffer)** receiving data cells from the direct memory access unit **(fig 1, 44 shows DMA)** in response to a second READY signal **(Col 3 lines 59-60 shows a request signal equivalent to a 2nd ready signal)** and exchanging control signals **(fig 2, 150 and 151 are control signals exchanged b/w the FIFO and DMA according to Col 4 lines 61-66)** with the direct memory access unit **(fig 1, 44 shows DMA)**; and an

output unit **(fig 1, 30 is equivalent to an output unit)**, the output unit **(fig 1, 30 is equivalent to an output unit)** receiving data cells from the output buffer unit **(fig 1, 40 is equivalent to buffer unit)** and applying data cells to the communication bus **(fig 1, 50 shows communication bus)**, the output unit **(fig 1, 30 is equivalent to an output unit)** exchanging UTOPIA format signals (**Jensen shows UTPOIA format signals in Col 1 lines 65-66**) with the ATM master processing unit **(fig 1, where 20 represents an ATM master processing unit similar to the one shown by Jensen)**.

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the slave devices of Jensen, as taught by Holm, since stated in Col 1 lines 41-45, that such a modification will alleviate the difficulty to place a large number of RAM's on a single integrated circuit and no longer limit the number of communication channels that can be supported on the integrated circuit.

Allowable Subject Matter

3. Claims 1, 4, 5, 7, 18 and 19 are allowed.

Response to Arguments

4. Applicant's arguments with respect to claims 10 and 14 have been considered but are moot in view of the new ground(s) of rejection.

5.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER P. GREY whose telephone number is (571)272-3160. The examiner can normally be reached on 10AM-7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Moe Aung can be reached on (571)272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
Supervisory Patent Examiner, Art Unit 2616

/Christopher P Grey/
Examiner, Art Unit 2616